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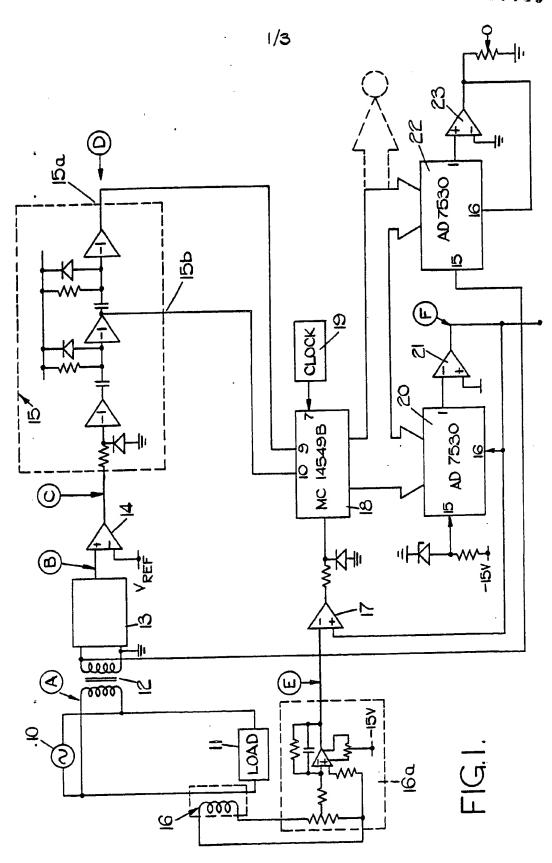
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(74) Agents Marks & Clerk Alpha Tower ATV Centre Birmingham B1 1TT may be multiplex operated to derive the power signal.

(54) Measurement of power in A.C. circuits

(57) An a.c. power measurement circuit includes a current transducer (16, 16a), a circuit (12, 13, 14) which detects the instant when the voltage is maximum by detecting the zero crossings in an a.c. waveform 90° out of phase with the voltage and a sampling circuit (18, 19, 20) which samples the output of the current transducer at the instant of the voltage peak. A digital to analog converter (22) is used as a multiplier to derive a power signal. Alternatively a similar converter (20) used in the sampling circuit

B C FIG. 1.



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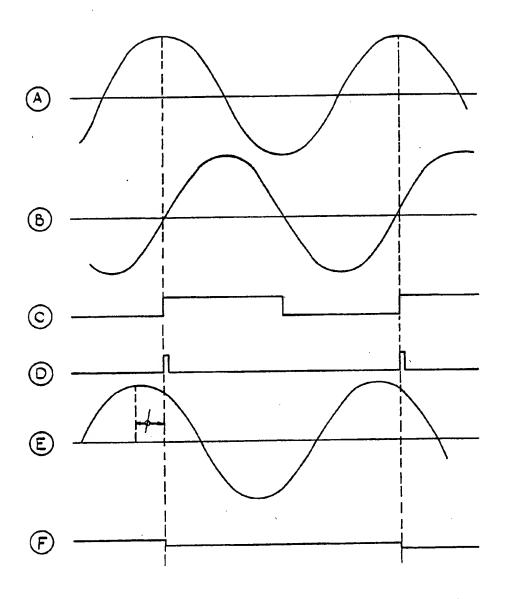
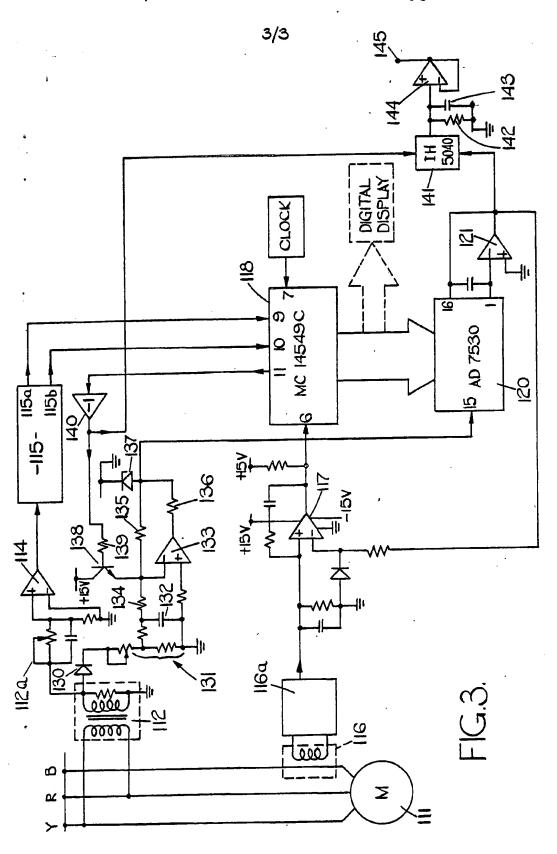


FIG.2.

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SPECIFICATION

Measurement of power in a.c. circuits

5 This invention relates to the measurement of power in a.c. circuits.

Generally speaking the power in an a.c. circuit is determined by the equation,

(a)

 $P = V.I. \cos \emptyset$ 10 where P is the power (in watts) V is the r.m.s. voltage I is the r.m.s. current (in amps) Ø is the phase angle between the and current and voltage waveforms.

When the current and voltage waveforms are both sinusoidal this equation can be rewritten as,

 $P = \frac{1}{2} Vp. ip. cos\emptyset$ where Vp is the peak voltage

Ip is the peak current (in amps). 20 and The present invention rests on the realisation that the value of the current at the instants when the voltage is at its peak value is equal to Ip cosØ thereby giving the oppor-25 tunity for a very simple method of power measurement which does not involve assess-

ing the phase angle between the current and

voltage waveforms.

According to one aspect of the invention 30 there is provided a method of measuring the power in an a.c. circuit in which both the current and voltage waveforms are sinusoidal (or substantially sinusoidal) in which the value of the product of the peak value of one of the 35 two variables consisting of the current and the voltage and the cosine of the phase angle is obtained by detecting the magnitude of the variable when the other variable is at its peak

40 Conveniently the detection of said other variable being at its peak level is carried out by detecting when an a.c. signal 90° out of phase with the other variable crosses zero.

The invention also resides in an apparatus 45 for use in carrying out the above defined method and comprising a transducer for producing a signal dependent on the instantaneous value of one of the two variables consisting of the current and the voltage, a peak

50 detector circuit for determining the instants when the other of said variables is at its peak -value, and sampling means for sampling said one variable under the control of said peak detector circuit.

55. In a single phase circuit said peak detector circuit may comprise a 90° phase shift circuit receiving a signal related to said other variable, and a zero crossing detector circuit receiving the output of phase shift circuit.

In a three-phase a.c. circuit (where direct measurement of the phase voltage may be impossible) the peak detector means may be a zero-crossing detector circuit receiving an input corresponding to the voltage difference 65 between two of the phase conductors, the

transducer measuring the current in the other phase conductor.

An example of the invention is shown in the accompanying drawings in which:-

Figure 1 is a block diagram of an apparatus for measuring a.c. power,

Figure 2 is a graph showing waveforms at various points in Fig. 1, and

Figure 3 is a diagram showing another 75 example of the invention intended for use in a three phase a.c. circuit.

Referring firstly to Fig. 1, an a.c. source 10 is connected to a load 11, the power dissipation in which it is desired to measure.

A transformer 12 has its primary winding connected across the load and its secondary winding connected to a 90° phase shift circuit 13 (it being assumed that the source 10 is of sensibly constant frequency). The output of

85 the circuit 13 is connected to the input of a zero-crossing detector circuit 14, the output of which is connected to a pulse generating circuit 15 which produces at an output terminal 15a a short duration output pulse each

90 time there is a positive-going transition in the output of circuit 14. The circuit 15 also has an output terminal 15b at which a short pulse is produced preceding the pulse at terminal 15a.

A current transformer 16 is associated with one of the conductors connecting the source 10 the load 11 is connected to an amplifier circuit 16a provides an output voltage proportional to the instantaneous value of the cur-

100 rent in that conductor. The output of circuit 16a is connected to the inverting input of a voltage comparator 17.

A successive approximation register 18 (Motorola integrated circuit type MC 14549B)

105 has its "data input" terminal connected to the output of comparator 17, its "master reset" terminal connected to the terminal 15b, its 'start conversion'' terminal connected to the terminal 15a and its "clock" terminal con-

110 nected to a clock pulse generator 19 running at a frequency sufficient to ensure that a complete conversion cycle can take place in a time very short compared to the time of a half cycle of the supply.

The eight-bit digital output of the register 18 is applied to the data inputs of a digital to analogue converter 20 (Intersil integrated circuit type AD 7530). The V_{REF} input of converter 20 is connected to a zener-regulated sup-

120 ply and its current output is connected to the inverting input of an operational amplifier 21. The output of amplifier 21 is connected to the $R_{\mbox{\tiny FEEDBACK}}$ terminal of converter 20 and also to the non-inverting input of the voltage compar-

125 ator 17.

The arrangement described operates as follows:--- When the positive-going zero-crossing of the output of the 90° phase shifter 13 occurs, the register 18 is first reset to zero by 130 the pulse from terminal 15b and the pulse at

terminal 15a then causes conversion to commence. In known manner, the output of the comparator 17 at each clock pulse determines the respective bits of the multi-bit digital out-5 put of the register 18, the comparator comparing the output of amplifier 21 (which is the re-converted analog signal) with the incoming analog signal from circuit 16a. At the end of the conversion cycle (i.e. eight clock pulses 10 the output of the amplifier 21 is the same as the signal from circuit 16a plus or minus the analog equivalent of the least significant bit of the register output.

Either the multi-bit digital signal or the 15 output of amplifier 21 may be used to drive a display or to provide an input to ancillary equipment (for example for power trip circuit). When the voltage of the supply is known to be constant, these signals provide a direct 20 indication of the power dissipation. When a digital display is used the pulse from terminal 15a is used in known manner for display blanking during conversion.

In cases where the voltage fluctuates it is 25 necessary to measure the voltage and multiply this by the Ip cos Ø term. In the example shown in the drawing this function is carried out by means of an additional digital to analog converter 22 together with an amplifier 30 23 connected in the same manner as converter 20 and amplifier 21, but with the VREF terminal of converter 22 connected to the output of the transformer 12. The output of the amplifier 23 is an a.c. signal in phase

35 with the output of voltage transformer 12 and of amplitude equal to Ip.Vp cosØ. This signal can either be applied to an a.c. meter or rectified and averaged in known manner to obtain the desired power indication.

It will be appreciated that in the case of a circuit in which there is no change in voltage the present invention provides a very simple arrangement for measuring the power, which does not involve measuring the phase shift Ø. 45 Even when the voltage is variable the circuit described is still substantially simpler than conventional circuits in which phase shift

measurement is necessary.

It will, of course, be understood that, al-50 though the above embodiment of the invention detects zero crossings in the phase-shifted voltage signal and samples current, it is also possible to detect zero-crossing in a 90° phase-shifted current signal and sample the 55 voltage signal.

Turning now to Fig. 3, a three phase supply is shown driving a three-phase load 111 such as a motor. A current transformer 116 with an associated circuit 116a provides an output 60 varying with the current in the B-phase conductor of the a.c. supply, components 116 and 116a corresponding precisely to the components 16 and 16a in Fig. 1. The signal from circuit 16 is fed, as before, to a voltage 65 comparator 117, but additional components

are now shown surrounding this comparator to improve its performance, but no detailed description of these components is considered necessary herein.

A transformer 112 has its primary winding connected between the Y- and R-phase conductors of the supply, the voltage difference between these conductors being 90° out of phase with the voltage on the B-phase con-

75 ductor. One end of the secondary winding of transformer 112 is earthed and the other is corrected via a phase correction network 112a to an amplifier 114 corresponding to amplifier 14 of Fig. 1. The output of amplifier 114 is

80 connected to a circuit 115 corresponding to circuit 15, with outputs 115a and 115b connected to the "START-CONVERSION" and "MASTER-RESET" input terminals of a successive approximation register 118, to the

85 "DATA INPUT" terminal of which the output of comparator 117 is connected. The eight bit digital output of register 118 is connected to the data inputs of the digital-to-analog converter 120 of which only one is used in the

90 present example, both for conversion of the input signal representing I cosØ and for analog multiplication by the voltage signal at different times in the cycle of operation.

To this end, the "other" end of the second-95 ary of transformer 112 is connected by a diode 130 and an adjustable resistor network 131 to a smoothing capacitor 132, such that the voltage stored on capacitor 132 is roughly equal to the average voltage at said other end

100 of the secondary winding. An operational amplifier 133 has its non-inverting input earthed and its inverting input connected by a resistor 134 to the capacitor 132. The inverting input is also connected by two resistors 135, 136

105 in series to the output terminal of amplifier 133, the junction of these resistors being connected by a zener diode 137 to earth. An npn transistor 138 has its emitter connected to the inverting input of amplifier 133, its

110 collector connected to the + 15V supply rail and its base connected by a resistor 139 to the output of a logical inverter 140 having its input connected to the "END of CONVER-SION" output terminal of the register 118.

115 The signal at this terminal goes low when conversion commences and stays low until conversion has ended. Thus, during conversion transistor 138 is conducting and drives the amplifier 133 output to nearly -15V,

120 irrespective of the voltage on capacitor 132. The signal applied to the reference voltage terminal of converter 120 is thus determined during this time by the zener diode 137.

When conversion is completed transistor 138 125 turns off and amplifier 133 then functions as a linear inverting amplifier controlling the reference voltage applied to the converter 120 in accordance with the voltage on capacitor 132.

To prevent the signals generated by conver-130 ter 120 during conversion from being passed

to the output of the circuit, a CMOS analog switch 141 (type IH 5040) is used. This has its signal input terminal connected to the output of operational amplifier 121 associated with converter 120, and its control input connected to the output of inverter 140. A resistor 142 and a capacitor 143 (having a time constant which is long in comparison to the cycle period) are connected in parallel 10 between the output of switch 141 and earth, a buffer amplifier 144 connecting the output of the switch 141 to the final output terminal

15 ČLAIMS

- 1. A method of measuring the power in an a.c. circuit in which both the current and voltage waveforms are sinusoidal (or substantially sinusoidal) in which the value of the 20 product of the peak value of one of the two variables consisting of the current and the voltage and the cosine of the phase angle is obtained by detecting the magnitude of the variable when the other variable is at its peak 25 level.
- 2. A method as claimed in claim 1 in which the detection of the peak level of said other variable is carried out by deriving an a.c. signal 90° out of phase with said other 30 variable and detecting zero crossings in said a.c. signal.

3. A method as claimed in claim 2 in which said a.c. signal is derived by phaseshifting a signal representing said other vari-

4. A method as claimed in claim 2 as applied to a three phase supply in which said other variable is the voltage of one phase, said a.c. signal being derived by detecting the 40 difference in voltage of the other two phases.

5. Apparatus for use in carrying out the method claimed in claim 1 comprising a transducer for producing a signal dependent on the instantaneous value of one of two variables 45 consisting of the current and the voltage, a

peak detector circuit for determining the instants when the other of said variables is at its peak value, and sampling means for sampling said one variable under the control of said

50 peak detector circuit.

6. Apparatus as claimed in claim 5 in which the peak detector circuit comprises means for generating an a.c. signal 90° out of phase with said other of said variables and a 55 zero-crossing detector detecting zero-crossings in said a.c. signal.

7. Apparatus as claimed in claim 6 in which said a.c. signal generating means com-

prises a 90° phase shifter circuit.

8. Apparatus as claimed in claim 6 in which said other of said variable is the voltage of one phase of a three phase supply and said a.c. signal generating means is sensitive to the difference in voltage of the other two 65 phases.

9. Apparatus as claimed in any of claims 5 to 8 inclusive in which said sampling means comprises an analog to digital converter which has a conversion time which is very short in 70 comparison to the a.c. cycle period.

10. Apparatus as claimed in claim 9 in which said analog to digital converter includes a successive approximation register, a digital to analog converter having its digital inputs

75 connected to the respective digital outputs of the register and a comparator connected to the output of the digital to analog converter and to the transducer and controlling the operation of the register.

80 11. Apparatus as claimed in claim 10 including a further digital-to-analog converter having its digital inputs connected to the respective digital outputs of the register and a reference voltage input connected to a circuit 85 which produces a signal corresponding to said other variable.

12. Apparatus as claimed in claim 10 including switch means controlled by the register for applying to a voltage reference termi-90 nal of the digital to analog converter a reference signal during the conversion time and a signal related to the value of said other variable at other times.

13. Apparatus as claimed in claim 12 95 further comprising an electronic switch device connecting the output of the digital to analog converter to an output terminal of the apparatus, said switch being controlled by the register so as to be open during conversion.

14. Apparatus as claimed in claim 13 100 further comprising a capacitor for storing the previous value of the electronic switch device output during conversion.

15. Apparatus for use in the measurement 105 of a.c. power substantially as hereinbefore described with reference to Fig. 1 of the accompanying drawings.

16. Apparatus for use in the measurement of a.c. power substantially as hereinbefore 110 described with reference to Fig. 3 of the accompanying drawings.

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